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## 1. Name of conveying party(ies):

Haruhiko MURATA, Yukihiro KIMURA and Masashi  
INAISHIAdditional name(s) of conveying party(ies) attached? No

## 2. Name and address of receiving party(ies):

Name: NGK SPARK PLUG CO., LTD.

Internal Address:

Street Address: 14-18, Takatsuji-cho, Mizuho-ku,  
AichiCity: Nagoya-shi, State: Japan ZIP: 467Additional name(s) & address(es) attached? No

## 3. Nature of conveyance:

☒ Assignment                      ☐ Merger  
☐ Security Agreement              ☐ Change of Name  
☐ Other ☐Execution Date: March 17, 1997

## 4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is: March 17,  
1997

A. Patent Application No.(s)

B. Patent No.(s)

Additional numbers attached? No

## 5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Richard L. SchwaabInternal Address: FOLEY & LARDNERStreet Address: 3000 K Street, N.W., Suite 500City: Washington, State: D.C. ZIP: 20007-51096. Total number of applications and patents involved: 17. Total fee (37 C.F.R. § 3.41). . . . . \$40.00☒ Enclosed☐ Authorized to be charged to deposit account8. Deposit account number: 19-0741

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## 9. Statement and signature.

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Name of Person SigningGeorge E. Quillen  
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1 581

March 28, 1997  
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# A S S I G N M E N T

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(hereinafter ASSIGNEE) all right, title and interest for the United States, its territories and possessions in and to his invention relating to

title of  
invention

IMPROVEMENT IN OR RELATING TO CIRCUIT BOARD HAVING SOLDER BUMPS  
as set forth in his/her United States Patent Application

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03/28/97

Assistant Commissioner for Patents  
Washington, D. C. 20231

Sir:

Transmitted herewith for filing is the patent application of:

**INVENTOR(S): Haruhiko MURATA, Yukihiro KIMURA and Masashi INAISHI**

**TITLE: IMPROVEMENT IN OR RELATING TO CIRCUIT BOARD HAVING SOLDER BUMPS**

In connection with this application, the following are enclosed:

- 40 Pages of Specification with Abstract
- 11 Claims
- 12 Sheets of Drawings
- XX Declaration, Power of Attorney
- XX Assignment to: NGK SPARK PLUG CO., LTD.
- XX Certified Priority Application and Priority Claim
- XX Preliminary Amendment
- XX Other: Check for \$810.00

The fee has been calculated as shown below. (Small entity fees indicated in parentheses.)

(1) For	(2) Number Filed	(3) Number Extra	(4) Rate	(5) Basic Fee \$770 (\$385)
Total Claims	11 - 20 =	0	x \$22 (x \$11)	0.00
Independent Claims	3 - 3 =	0	x \$80 (x \$40)	0.00
Multiple Dependent Claims			\$260 (\$130)	0.00
Assignment Recording Fee			\$ 40	40.00
			<b>TOTAL FEE:</b>	<b>\$810.00</b>

A check in the amount of the above TOTAL FEE is attached. This amount is believed to be correct; however, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 19-0741.

Respectfully submitted,

Date: March 28, 1997  
Docket No.: 040679/0439

*George E. Quillen 32,792*  
for Richard L. Schwaab  
Reg. No. 25,479

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No. 040679/0439

In re patent application of

Haruhiko MURATA et al.

Serial No. Unassigned

Filed: March 28, 1997

For: IMPROVEMENT IN OR RELATING TO CIRCUIT BOARD  
HAVING SOLDER BUMPS

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Prior to examination of the above-identified application, Applicants respectfully request that the following amendment be entered into the application:

IN THE SPECIFICATION:

Page 9, line 27, delete "Fig. 11 is an illustration" and insert "--Figs. 11A and 11B are illustrations--".

REMARKS

The Examiner is respectfully requested to enter the above amendments prior to examination of the instant application. The amendments are made to correct clerical and grammatical errors and are not deemed to change the scope of the invention.

Respectfully submitted,

March 28, 1997

for George E. Quillen 72 792  
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IMPROVEMENT IN OR RELATING TO CIRCUIT BOARD HAVING SOLDER  
BUMPS

BACKGROUND OF THE INVENTION

5 1. Field of the Invention

The present invention relates to a circuit board having solder balls or bumps such as for flip-chip bonding and ball grid array. Further, the present invention relates to a method of producing such a circuit board. Still  
10 further, the present invention relates to a flattening and leveling jig used for carrying out the method.

2. Description of the Related Art

In case of mounting, for example, an integrated circuit chip on an integrated circuit board, it is known  
15 to form on their joining surfaces a plurality of terminals of a grid pattern or checkered pattern and bond them by way of the terminals, i.e., a technology that is called flip chip.

Further, it is also known, in case of joining an  
20 integrated circuit board having installed thereon an integrated circuit chip to a printed circuit board such as a motherboard, a bonding technology of forming on a back surface of the integrated circuit board (i.e., a joining surface opposite to the front surface on which the  
25 integrated circuit chip is installed) a plurality of terminals which are bonding balls of high melting point solder, Cu or the like and arranged so as to form a grid pattern, for thereby bonding the integrated circuit board to the printed circuit board, such a board being called a  
30 ball grid array (BGA) board.

Various technologies such as a solder paste technology are known for forming such an integrated circuit

board or the like having terminals adapted for surface-to-surface joining and arranged so as to form a grid or checkered pattern.

For example, as shown in Fig. 15A, the solder paste technology includes a process of applying solder paste onto  
5 conductive base pads formed on an integrated circuit board by printing and thereafter melting the paste by heating for thereby forming semi-spherical or spherical solder bumps on the pads.

10 However, forming the solder bumps in the above described manner includes problems described hereinafter and improvement thereof has been eagerly required.

(1) Generally, it has been considered desirable that solder bumps formed on an integrated circuit board are equal  
15 in height to each other for the purpose of improving the joining or bonding ability or the like to be joined or bonded to the integrated circuit chip or the printed circuit board. That is, as shown in Fig. 15B, it has been considered desirable that the coplanarity "d" of all of the solder  
20 bumps "p" is small.

In this connection, the term "coplanarity" is expressed or represented by the distance "d" between two parallel surfaces S1 and S2 between which the tops or apices of all the solder bumps "p" are included, and is used as  
25 an index for indicating the irregularity in the height or level of the solder bumps. In this invention, a coplanarity per unit length, which is obtained by dividing the coplanarity by the maximum distance between the solder bumps (i.e., normally, the diagonal distance of the area  
30 in which the solder bumps are formed) since the coplanarity depends on the area in which the solder bumps are formed.

However, the height of each solder bump of itself varies depending upon the volume of solder applied to each pad and the size of the pad, etc., so that a variation in the volume of solder, the size of the pad, etc. causes the solder bumps to become irregular in height. Accordingly, there is caused a problem in that the coplanarity becomes larger. A further problem is that even if the solder bumps are equal in height a large coplanarity results in case the board is warped or curved.

When the coplanarity is large, a joining defect may possibly be caused since the distance between the terminals standing opposite to each other becomes irregular at the time of joining the integrated circuit board to the integrated circuit chip or the printed circuit board.

Further, even in case a probe is made to contact respective solder bumps with a view to examining the conduction of the conductors and the insulation between the conductors, it becomes difficult for the probe to contact predetermined solder bumps or all the solder bumps at the same time, so there occurred a case in which accurate measurement could not be obtained.

(2) An image processor is used for measurement of the coplanarity of the solder bumps for the purpose of examining the joining ability of the integrated circuit board but includes a problem in that since the top of the solder bump is constituted by a curved surface it is difficult to detect the highest point or apex of the solder bump and it is inevitable to set at least three points to which a laser beam is irradiated even in the case the highest point (apex) is obtained by approximation, causing a problem in that much labor is required.

#### SUMMARY OF THE INVENTION



According to an aspect of the present invention, there is provided a circuit board which comprises a substrate having a joining surface, and a plurality of solder bumps disposed on the joining surface of the substrate in such a manner as to form a predetermined profiled line or surface pattern, wherein the solder bumps have tops which are flattened and leveled, and a coplanarity of the solder bumps is  $0.5\text{ }\mu\text{m}$  or less per 1 mm. In this connection, the term "solder" is herein used to mean or indicate Pb-Sn based soft solder and other low melting point solders in a broad sense, such as Au-Sn solder, Au-Si solder, etc. Further, the term "circuit board" is intended to indicate not only (1) a board on which an integrated circuit chip is mounted but (2) a board to be joined with a printed circuit board and (3) an integrated circuit chip of itself (i.e., flip chip). More specifically, indicated by that term are (1) a board having, at one side surface thereof, a plurality of solder bumps for joining to an integrated circuit chip or chips (flip chip bonding), (2) a board having, at one side surface thereof, a plurality of solder bumps (usually, BGA), for joining to a printed circuit board, and (3) an integrated circuit chip having a plurality of solder bumps. The above described profiled line pattern is for example a square frame-like pattern. The profiled surface pattern is for example a grid pattern or checkered pattern.

According to a further aspect of the present invention, circular pads are interposed between the solder bumps and the substrate to serve as base layers of the solder bumps.

According to a further aspect of the present invention, the tops of the solder bumps have nearly circular flat surfaces which are smaller in diameter than the pads.

According to a further aspect of the present invention, the tops of the solder bumps have nearly circular flat surfaces which are substantially equal in diameter to the pads, and the height of the solder bumps is smaller than the diameter of the pads.

According to a further aspect of the present invention, there is provided a method of producing a circuit board including a substrate having a joining surface, and a plurality of solder bumps disposed on the joining surface of the substrate in such a manner as to form a predetermined pattern, wherein the solder bumps have tops which are flat and leveled, and a coplanarity of the solder bumps is 0.5  $\mu\text{m}$  or less per 1 mm. The method comprises the steps of placing masses of solder on the solder bumps, respectively, disposing a control member in the form of a flat plate at a predetermined position above the masses of solder, and forming the masses of solder into the solder bumps all at once by melting the masses of solder and allowing the control member to control the height of the solder bumps while flattening the tops of the solder bumps all at once. The above described solder material can be solder paste, solder preform, solder ball, one having been already formed into solder bump, or the like. The material for the above described control member can be a metal such as titanium and stainless steel, ceramics such as alumina, silicon nitride and silicon carbide, glass and the like, and such one that is not wetted by solder or has a difficulty in being wetted by solder is suitable therefor. Particularly, ceramics are suitable on the working accuracy and in that

its deformation by heat is small. The control member is a member for flattening the tops of the solder bumps while leveling the same, so it is desirable, for example, to provide to the opposite ends of a flat or planar plate with  
5 a pair of leg members so as to form an assembly having a U-like cross section since it becomes possible to control or adjust the level of the solder bumps through adjustment of the length or height of the leg members and furthermore the workability is improved. The temperature for melting  
10 the above described solder is required only to be equal to or higher than the melting point of the solder bump (i.e., the melting point of the solder) and, for example, can be higher than the melting point by 10 to 40 °C.

According to a further aspect of the present  
15 invention, in the above described method a plurality of pads are disposed on the joining surface of the substrate in such a manner as to form a predetermined profiled line or surface pattern, and the solder bumps are once formed on the pads, respectively and then pressed in such a manner as to allow  
20 the tops to be flattened and leveled. In carrying out the above described pressing, there are two cases, i.e., one in which a pressing portion of a pressing device is heated by a heater and the other in which the pressing portion is no heated. Of those, the case of heating is suitable since  
25 excessive stress does not result and solder bumps having smooth outer surface can be formed. In the meantime, in this instance, it is desirable to carry out the pressing in nonoxidizing atmospheres in order to prevent oxidation of the solder due to heating.

30 According to a further aspect of the present invention, in the above described method a plurality of pads are disposed on the joining surface of the substrate in such

a manner as to form a profiled line or surface pattern, and the solder bumps are once formed on the pads, respectively and then ground in such a manner as to allow the tops to be flattened and leveled. As a means for carrying out such grinding, a grinding machine having a rotary grinding wheel, for instance, can be used.

According to a further aspect of the present invention, there is provided a flattening and leveling jig for disposition above solder materials mounted on a main surface of a circuit board for controlling the height of solder bumps into which masses of solder are formed by being heated and molten. The jig comprises a control member having a planar surface for controlling the height of the solder bumps, and a pair of leg members which are independent parts and disposed on the side of the planar surface of the control member for support of the control member and for positioning of the planar surface. The material for the above described control member can be a metal such as titanium and stainless steel, ceramics such as alumina, silicon nitride and silicon carbide, glass and the like, and such one that is not wetted by solder or has a difficulty in being wetted by solder is suitable therefor. Particularly, ceramics are suitable on the working accuracy and in that its deformation by heat is small.

According to a further aspect of the present invention, in the above described jig the leg members are so constructed and arranged as to allow the planar surface of the control member to be parallel to the main surface of the substrate when the flattening and leveling jig is disposed in place.

According to a further aspect of the present invention, in the above described jig the leg members are made of wire rod. Such wire rod can be round or square rod.

According to a further aspect of the present invention, in the above described jig the control member has on the side of the planar surface a pair of grooves in which the leg members are fitted.

The above described circuit board, method of producing such a circuit board and a jig used in carrying out the method are useful and effective for solving the above noted problems inherent in the prior art device.

It is accordingly an object of the present invention to provide a novel and improved circuit board having a plurality of solder bumps, which can decrease the coplanarity of the solder bumps assuredly while simplifying measurement of the coplanarity.

It is a further object of the present invention to provide a novel and improved method of producing a circuit board of the foregoing character.

It is a yet further object of the present invention to provide a jig used for carrying out the method of producing a circuit board of the foregoing character.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

Fig. 1A is a perspective view of a circuit board having solder bumps according to example 1 of the present invention;

Fig. 1B is an enlarged, fragmentary sectional view of the circuit board of Fig. 1A;

Fig. 2A is an illustration of process steps for producing solder bumps;

Fig. 2B is an illustration of an effect obtained by the process of Fig. 2A;

Fig. 3 is an illustration of a process of producing solder bumps according to example 2 and example 3 of this invention;

Fig. 4A is a sectional view of a solder bump before  
5 processed by pressing;

Fig. 4B is a view similar to Fig. 4A but shows the solder bump after processed by pressing according to example 2;

Fig. 4C is a view similar to Fig. 4A but shows the  
10 solder bump after processed by pressing according to example 3;

Fig. 5 is an illustration of a process of producing a solder bump according to example 4 of this invention;

Fig. 6 is an illustration of an effect of this  
15 invention, i.e., the solder bump increasing in height at the time of melting;

Fig. 7 is an illustration of another effect of this invention, i.e., how the solder bumps are joined to the other of the joining pair;

Fig. 8 is a further effect of this invention, i.e.,  
20 the difference in the flattened degree of the tops of the solders;

Fig. 9 is an illustration of a further effect of this invention, i.e., how a solder ball is produced;

Fig. 10 is an illustration of a further effect of this  
25 invention, i.e., how a solder bridge is produced;

Fig. 11 is an illustration of how the volume of a solder bump is calculated;

Fig. 12A is a sectional view of a flattening and  
30 leveling jig according to example 5 of this invention;

Fig. 12B is a bottom plan of the leveling jig of Fig. 12A;

Fig. 12C is a side elevation of the leveling jig of Fig. 12A;

Fig. 13A is an elevation of a flattening and leveling jig according to a comparative example;

5 Fig. 13B is a bottom plan view of the flattening and leveling jig of Fig. 13A;

Fig. 13C is a side elevation of the flattening and leveling jig of Fig. 13A;

10 Figs. 14A is a sectional view of a variant of the flattening and leveling jig of Figs. 12A to 12C;

Fig. 14B is a side elevation of the flattening and leveling jig of Fig. 14A; and

Figs. 15 A and 15B are illustrations of a prior art.

#### DETAILED DESCRIPTION OF THE PREFERRED EXAMPLES

15 According to an aspect of the present invention, solder bumps of a circuit board are flattened and leveled. Accordingly, the number of points to which a laser beam is irradiated for measurement of the coplanarity of the circuit board can be reduced (e.g., one point will suffice),  
20 and therefore the efficiency of work can be improved considerably.

Further, the process of flattening the tops of the bumps also contributes to decrease of the coplanarity, as will be described hereinafter. For example, in the case a  
25 circuit board having solder bumps and an integrated circuit chip or a printed circuit board are disposed so as to stand opposite to each other, the solder bumps are brought completely into contact with the pads or the like of the integrated circuit chip or printed circuit board, or come  
30 closer thereto and into a position where the solder bumps and the pads can be soldered. Further, when the solder bumps

are reflowed, they are increased in height , i.e., the level of the tops of the solder bumps becomes higher.

This is because a mass of solder which tends to become spherical by nature, is pressed down to have a flat or planar portion as shown in Fig. 6, so it tends to become spherical once again when the mass of solder is reflowed at the time of joining and resultantly the solder bumps increase in height.

Accordingly, even when the circuit board of this invention and a mating board (i.e., semiconductor element, motherboard, or the like) are placed one upon another for joining to cause the pads of the mating board and the solder bumps of the circuit board of this invention to be out of contact due to the fact that the coplanarity of the pads of the mating board is so bad, i.e., large, the tops of the solder bumps are caused to go upward or become higher in level and thereby brought into contact with the pads by reflowing the solder bumps at the time of joining, so that a joining defect is hard to occur and an excellent joining ability can be obtained. In the meantime, the coplanarity of the mating board is about 10  $\mu\text{m}$  in case the mating board is an integrated circuit element and about 100  $\mu\text{m}$  in case the mating board is a motherboard, so they can be joined assuredly, provided that the solder bumps can increase in height by the amount larger than that coplanarity at the time of joining.

Further, in the case the coplanarity is small, a probe in a conduction or insulation test can contact a predetermined solder bump or bumps, or all of the solder bumps, thus making it possible to carry out the test assuredly.



Description will be made hereinafter with respect to the size and characteristics of the flat or planar portions of the solder bumps.

(1) A larger diameter of the flattened portion is more  
5 desired.

This is because at the time of the solder being melted the solder tends to become spherical due to the surface tension, so the larger the flattened portion becomes (i.e., the more the solder bumps is depressed downward or  
10 flattened), the more the tops of the solder bumps increase in height at the time of joining in which the solder bumps are reflowed.

Fig. 8 shows examples (a), (b) and (c) having various flat tops, i.e., flat tops which differ in the degree of  
15 being flattened. As seen from Fig. 8, the solder bump which is flattened more so as to be lower in height, have a larger flattened portion at the top ( $a < b < c < d$ ). At the time when the solder bumps are reflowed, all the shapes (b), (c) and (d) of the solder bumps in Fig. 8 return to the shape  
20 (a), so that the solder bumps (b), (c) and (d) increase in height by the amount different in height from the bump (a) (with respect to increase in height,  $a < b < c < d$ ). Accordingly, as the flattened portion becomes larger, the tops of the solder bumps go much nearer to the pads or the  
25 like of the mating board which is an object to be joined, at the time of joining, so even if the coplanarity of the circuit board of this invention or the surface property of the mating board is bad, their joining can be attained with ease.

(2) The diameter of the flattened portion is desired  
30 to be equal to or smaller than the result of the diameter of a solder bump base pad  $\times 1.5$ .

This is because, as shown in Table 1, when the diameter of the flattened portion becomes larger than 1.5 times as large as the diameter of the solder bump base pad, a part of the solder not located on the pad but bulging out therefrom is separated from the remainder to drop and form a solder ball or balls, so that the resulting solder balls may possibly stick or adhere to the board so as to connect between the pads and deteriorate the insulation ability. In the meantime, in Table 1, the relation between the diameter of the flattened portion of the solder bump and the percentage of solder ball production is shown.

Table 1

Diameter of flattened Portion	Production Rate of solder Ball
150 $\mu\text{m}$ (Pad Dia. x 1.00)	0/10000 Pads ( 0 %)
188 $\mu\text{m}$ (Pad Dia. x 1.25)	0/10000 Pads ( 0 %)
225 $\mu\text{m}$ (Pad Dia. x 1.50)	0/10000 Pads ( 0 %)
263 $\mu\text{m}$ (Pad Dia. x 1.75)	1000/10000 Pads (10 %)
300 $\mu\text{m}$ (Pad Dia. x 2.00)	5000/10000 Pads (50 %)

In the Table, the diameter of the solder bump base pad is 150  $\mu\text{m}$ , and the height of the solder bump is 50  $\mu\text{m}$ .

(3) The diameter of the flattened portion is desired to be equal to or smaller than the result of pad diameter x 0.5.

This is because the flattened portion of the solder bump may be protruded radially outward of the solder bump base pad when flattened and have a possibility of developing, when protruded too much, a short circuit between it and the solder bump of its adjacent pad at the

time of joining, as shown in Table 2 and in Fig. 10. In the meantime, in Table 2, the relation between the diameter of the flattened portion of the solder bump and the production rate of solder bridge between solder bump base pads at the time of joining is shown.

Table 2

Diameter of flattened Portion	Production Rate of Solder Bridge between pads at the time of joining
150 $\mu\text{m}$ (Pad Dia. + Distance between Pads x 0.0)	0/1000 Pads ( 0 %)
180 $\mu\text{m}$ (Pad Dia. + Distance between Pads x 0.3)	0/1000 Pads ( 0 %)
200 $\mu\text{m}$ (Pad Dia. + Distance between Pads x 0.5)	0/1000 Pads ( 0 %)
220 $\mu\text{m}$ (Pad Dia. + Distance between Pads x 0.7)	2000/1000 Pads (20 %)
250 $\mu\text{m}$ (Pad Dia. + Distance between Pads x 1.0)	Solder Bridge being produced in All of Pads at the time of flattening of Solder Bump

In Table 2, the diameter of the solder bump base pad is 150  $\mu\text{m}$ , and the height of the solder bump is 50  $\mu\text{m}$ .

(4) The diameter of the flattened portion is desired to be 50  $\mu\text{m}$  or more from a point of view of image processing.

This is because if the flattened portion is so sized as to be equal to or larger than 150  $\mu\text{m}$  in diameter, though the diameter differs depending upon an image processor used, the flattened portion of the solder bump can be recognized assuredly by means of an image processor and the coplanarity can be measured automatically by means of a three-dimensional laser measuring device. The relation between the diameter of the flattened portion of the solder bump and the occurrence rate of error recognized by an image processor is shown in Table 3.

Table 3

Diameter of Flat Portion	Occurrence Rate of Error recognized by Image Processor	
	Image Processor of Company A's make	Image Processor of Company B's make
20 $\mu\text{m}$	100/100 (100 %)	70/100 (70 %)
30 $\mu\text{m}$	40/100 ( 40 %)	20/100 (20 %)
40 $\mu\text{m}$	5/100 ( 5 %)	0/100 ( 0 %)
50 $\mu\text{m}$	0/100 ( 0 %)	0/100 ( 0 %)
60 $\mu\text{m}$	0/100 ( 0 %)	0/100 ( 0 %)

In Table 3, the diameter of the solder bump base pad is 150  $\mu\text{m}$ , and the height of the solder bump is 50  $\mu\text{m}$ .

Accordingly, considering that the above described (1) to (4) are allowable limits, it may safely be said that  
5 the diameter of the flattened portion is within the range of the pad diameter  $\times$  (0.5 to 1.2).

More specifically, in the case the pad diameter is 150  $\mu\text{m}$  and the distance between pads is 100  $\mu\text{m}$ , the allowable diameter of the flattened portion is in the range  
10 of 50 to 200  $\mu\text{m}$ , and the optimum diameter of the flattened portion is in the range of 75 to 180  $\mu\text{m}$ .

According to another aspect of the present invention, the coplanarity of the solder bumps per 1 mm is set to be 0.5  $\mu\text{m}$  or less, so it becomes possible to join the circuit  
15 board of this invention to an integrated circuit chip, printed circuit board or the like favorably while becoming possible to perform a conduction test, insulation test and the like accurately.

Since the coplanarity per 1 mm is set to be 0.5  $\mu\text{m}$   
20 or less according to the present invention, it becomes possible to join, in case of joining the circuit board of this invention to an integrated circuit chip or a printed

circuit board such as motherboard, the solder bumps to the pads formed in the mating chip or printed circuit board assuredly.

According to a further aspect of the present invention, the diameter of the flattened portion of the solder bumps is set to be nearly equal to the diameter of the solder bump base pad.

Since the solder bumps are flattened at the top according to the present invention, they tend to become spherical and become higher in level at the tops when heated to reflow, and are thus brought into contact with the mating pads to be joined thereto, even if the tops of the solder bumps should be spaced away from the pads or the like of the integrated circuit or the printed circuit board. Particularly, the solder bump which is pressed down and deformed to such an extent that the flattened top of the diameter nearly equal to the diameter of the solder bump base pad is obtained, can effect large increase in height and is therefore excellent in the joining ability.

In the meantime, if the solder bumps are flattened excessively so that the flattened portion becomes larger in diameter than the bump base pad to bulge out therefrom, there may possibly occur such a case in which the bulged out part of the solder bump is separated from the remainder to form a solder ball or balls and deteriorate the insulation property or to cause a solder bridge or bridges between the adjacent pads to develop a short. However, since the diameter of the flattened portion is set substantially equal to that of the bump base pad according to the present invention, there is not produced any defective circuit board in which a solder ball or solder

bridge is caused, and therefore the circuit board of this invention is excellent in the joining ability.

According to a further aspect of the present invention, the diameter of the flattened portion of the solder bump is set nearly equal to that of the solder bump base pad, and the height of the solder bump is set smaller than the diameter of the solder bump base pad.

That is, since the solder bumps are shaped flat at the top according to the present invention, they tend to become spherical and become higher in level at the tops when heated to reflow, and are thus brought into contact with the mating pads to be joined thereto, even if the tops of the solder bumps should be spaced away from the pads or the like of the integrated circuit chip or the printed circuit board. Particularly, the solder bump having a diameter nearly equal to that of the solder bump base pad and the height smaller than the diameter of the solder bump base pad, can effect large increase in height and is therefore excellent in the joining ability. In Table 4, the relation between the height of the solder bump and the increase in height of the solder bump at the time of joining, in case the flattened portion and the solder bump base pad are equal in diameter is shown.

25

Table 4

Height of Solder Bump	Height of Solder Bump at the time of Reflowing	Increase in Height of Solder Bump at the time of Reflowing
50 $\mu\text{m}$	80 $\mu\text{m}$	30 $\mu\text{m}$
100 $\mu\text{m}$	130 $\mu\text{m}$	30 $\mu\text{m}$
150 $\mu\text{m}$	178 $\mu\text{m}$	28 $\mu\text{m}$
200 $\mu\text{m}$	223 $\mu\text{m}$	23 $\mu\text{m}$
250 $\mu\text{m}$	271 $\mu\text{m}$	21 $\mu\text{m}$

In Table 4, the diameter of the solder bump base pad is 150  $\mu\text{m}$ , and the diameter of the flattened portion is 150  $\mu\text{m}$ .

5 If the solder bump is flattened excessively so that the diameter of the flattened portion becomes larger than that of the solder bump base pad to bulge out therefrom too much, there may possible occur such a case in which the bulged-out part of the solder bump is separated from the remainder to form a solder ball or balls to deteriorate the insulation property or a solder bridge or bridges between  
10 the adjacent pads to develop a short. However, since the diameter of the flattened portion is set nearly equal to that of the bump solder base pad according to the present invention, there is not produced any defective circuit  
15 board in which a solder ball or solder bridge is caused, and therefore the circuit board of this invention is excellent in the joining ability.

The above described solder bump according to the present invention can be formed with ease by setting the  
20 amount of solder to be applied to a suitable value (in case of screen printing, it can be set depending upon the opening diameter of the metal mask and its thickness) since the volume of the solder bump can be obtained from the following expression (1), and by flattening the solder bump so that  
25 a desired height of the solder bump is obtained. Further, since it can be calculated from the following expressions (1) and (2) how much the height of the solder bump is increased at the time of reflowing of the solder bump for joining, a desired shape of the solder bump can be obtained  
30 by calculation depending upon how much the height of the solder bump is required to increase at the time of joining,

and therefore an advantage is that the design of product can be attained with ease.

The volume S of the solder bump at the time of flattening is obtained by:

5           
$$S = (r^2 \times T + T^3/6) \times \pi \quad \cdots (1)$$

where T = the height of the solder bump and r = 1/2 of the diameter of the flattened portion of the solder bump at the time of joining.

10           The volume S of the solder bump at the time of reflowing is obtained by:

$$S = (2 \times L^3 + 3 \times L^2 \times t - t^3) \times \pi/3 \quad \cdots (2)$$

15           where  $L^2 = r^2 + t^2$ ,  $\pi$  = the ratio of the circumference of a circle to its diameter, t = the distance between the bottom and the center of the solder bump, L = the diameter of the solder bump at the time of reflow, and r = 1/2 of the diameter of the solder bump base pad.

20           According to a further aspect of the present invention, after a plurality of masses of solder are placed respectively on a plurality of solder bumps which are disposed on a joining surface of a substrate so as to form a profiled line or surface pattern, a control member is disposed at a predetermined height control position above the masses of solder (i.e., at a position for controlling the height of the solder bumps all at once at the time of  
25           melting of the solder) for forming a flat or planar surface which is distant a predetermined amount from the joining surface of the substrate, and the solder masses are formed into the solder bumps which are flat or planar at the tops, by being heated and melted.

30           That is, since the masses of solder is heated and melted under the condition in which the flat or planar surface of the control member is disposed in such a manner



that the height of the masses of solder (i.e., the height of the solder bumps to be formed) does not become larger than a predetermined value and the tops of the solder bumps become flat or planar while the coplanarity becoming  
5 smaller.

In this instance, even if the circuit board is slightly curved, such a curvature is absorbed through adjustment of the height of the solder bumps controlled by the flat or planar surface of the control member, so an  
10 advantage from this point is that the coplanarity becomes smaller.

Accordingly, by using a jig of a simple structure and by a simple means of performing the flattening at the time of melting of solder, it becomes possible to produce a  
15 circuit board having solder bumps which are suitable and desirable for joining, without increasing the number of working steps and requiring equipment investment. Particularly, in the case a jig in the form of a flat plate with legs and having a U-like cross section, the height of  
20 the solder bumps is determined by the length or height of the legs, and therefore an advantage is that the work can be done under a stable condition.

Further, though generally the solder is oxidized with ease, melting of the solder is usually carried out in  
25 nonoxidizing atmospheres, so the degree of oxidization is small and a high joining ability can be maintained even in the case the solder is reflowed at the time of joining of the circuit board to an integrated circuit chip or printed circuit board.

30 According to a further aspect of the present invention, a plurality of solder bumps which are flat or planar at the tops are formed by once forming the solder

bumps respectively on a plurality of pads which are disposed on a joining surface of a substrate of a circuit board so as to form a profiled line or surface pattern, and then pressing the solder bumps so as to be leveled at the tops.

5        In carrying out such pressing, there are two cases, i.e., one in which a pressing portion of a pressing device is heated by a heater and the other in which the pressing portion is not heated. Of those, in the case of the pressing portion being heated, the solder is softened and melted,  
10       thus preventing generation of excessive stress while restraining oxidation due to stresses caused by pressing, so that it becomes possible to flatten the tops of the solder bumps smoothly. On the other hand, in the case of cold pressing, the heater for heating is unnecessary, so the tops  
15       of the solder bumps can be flattened with ease. That is, it becomes possible to produce a circuit board having solder bumps which are suitable for joining by a simple means, i.e., pressing.

         According to a further aspect of the present  
20       invention, a plurality of solder bumps which are flat or planar at the tops are formed by once forming solder bumps respectively on a plurality of pads which are disposed on a joining surface of a substrate in such a manner as to form a profiled line or surface pattern, and then grinding the  
25       solder bumps in such a manner that the tops of the solder bumps are flattened and leveled. That is, only by grinding by means of a grinder or the like grinding machine, it becomes possible to make the tops of the solder bumps flat or planar and it becomes possible to produce a circuit board  
30       having solder bumps which are suitable for joining.

         In the meantime, whether the flat or planar tops of the solder bumps are produced by melting, pressing or

grinding can be distinguished one from the other by inspection of the surface, cross section, etc.

According to a further aspect of the present invention, a flattening and leveling jig has a control member having a flat or planar surface for controlling the height of the solder bumps and a pair of leg members which are independent parts from the control member, for supporting the control member and controlling the position of the flat or planar surface of the control member.

It is not easy to manufacture a flattening and leveling jig having a control portion and leg portions integral with the control portion and protruding from the flat surface thereof, by grinding a material which is difficult to be cut or machined, such as ceramics. Particularly, it is difficult to maintain the flatness of the flat or planar surface at a high level.

Thus, according to the present invention, the control member and the leg members are formed from independent parts so that the manufacture of the jig can be easy. That is, in case of the jig of this invention, the control member can be formed or produced solely or independently, so it becomes possible to use as a material for the flattening and leveling jig for flattening the tops of the solder bumps, ceramics or the like which are suitable in that, for example, ceramics are small in the coefficient of thermal expansion and solders do not stick or adhere to the ceramics with ease. Furthermore, the process of making higher the flatness of the flat or planar surface of the control member can be done with ease since the control member can be processed under a condition of not being provided with the leg members. Further, regarding the leg members, the material for the leg members can be selected by

consideration on only the characteristics or properties required for the leg members, so an advantage is that not only the manufacture of the flattening and leveling jig can be easy but the manufacturing cost of the circuit board can be decreased. That is, it is not necessary for the leg members to be considered about the sticking or adhering property with respect to solder, so it is not necessary for the leg members to be made of ceramic, and therefore a metal which is easy in working or machining and cheap can, for example, be used as the material for the leg members.

According to a further aspect of the present invention, the flattening and leveling jig has the leg members which are constituent parts independent from the control member and constructed and arranged so as to allow the planar surface of the control member to be parallel to the main surface or joining surface of the substrate when the flattening and leveling jig is disposed in place. Accordingly, by disposing the control member on the substrate by way of the leg members, the flat surface of the control member becomes parallel to the main surface or joining surface of the substrate, so the tops of the solder bumps are formed with flat surfaces parallel to the joining surface of the substrate.

According to a further aspect of the present invention, wire or wire rod can be used as a material for forming the leg members of the flattening and leveling jig. The wire rod can be a round rod or square rod. Particularly, round wire rod can be obtained and worked with ease, and it is also easy to get a round wire rod of high precision.

According to a further aspect of the present invention, the control member has on the flat surface side a pair of grooves in which the leg members are fitted. Thus,

the positioning and fixing of the leg member can attained with ease since it only requires to dispose the leg members in the grooves. Further, the distance between the control member and the circuit board (i.e., the height of the solder bump) can be set variously through adjustment of the depth of the grooves.

Generally, the minimum limit of the diameter of a fine wire which is uniform in diameter and has a desired strength is about 0.3 mm, so in the case of the necessity of forming solder bumps of the height smaller than such a minimum diameter it can be met by forming grooves in the ceramic plate by grinding and fitting the fine wire in the grooves.

In the meantime, the machining for forming grooves in the ceramic material is easy as compared with the machining for forming a projection in the ceramic material, particularly from the point of view of the flatness of the flat surface required to be maintained high, the area to be machined, and the like.

A circuit board and its production method according to the present invention will be described further with respect to examples.

#### Example 1

In this example, a top of a solder bump is flattened and leveled at the time of melting of the solder bump.

In the meantime, description is herein made as to a resinous integrated circuit board for use in mounting thereon an integrated circuit chip (hereinafter referred to simply as circuit board), i.e., a circuit board having solder bumps used for connecting thereto an integrated circuit chip by a flip-chip technology.

As shown in Fig. 1A, a circuit board 3 of this example is a resinous board which is about 25 mm square and about 1 mm thick.

(1) In production of the circuit board 3, as shown in Fig. 1B, insulation layers 7 made of epoxy resin are first formed on a BT (bismaleimide triazine resin) core layer 5 to constitute a substrate, while Cu inner conductive pathways 9 through the insulation layers 7 and the BT core layer 5 being formed by a semi-additive process using a Cu electroless plating or Cu electroplating, and laminated one upon another on the core layer 5. In the meantime, the process of forming the Cu inner wiring can be performed by a subtractive process or a full additive process.

(2) Then, on the outermost surface of the circuit board 3, an about  $3\mu\text{m}$  thick Ni-P layer 13 is formed by Ni-P electroless plating for a Cu conductive pathway 11 joined with the Cu inner conductive pathways 9 to be resistance to corrosion and for improving the adhering quality of the same. Further on the Ni-P layer 13, an about  $0.1\mu\text{m}$  thick Au layer 15 by Au electroless plating is formed for thereby constituting a base conductive pad or solder bump base pad 17 consisting of the Ni-P layer 13 and the Au layer 15. In the meantime, in other places, a solder resist layer 19 of acrylic resin or epoxy resin is formed.

In the meantime, the above described plating process is the same as a well-known plating process used for a multi-layer printed circuit board as for example disclosed in "365 steps for Multi-layer Printed Circuit Board" written by Fujihira and Fujimori and published by Association of Industrial Research, so the detailed description thereto is omitted for brevity.

(3) Then, as schematically shown in Fig. 2A, on the pad 17 formed on the surface (joining surface) of the circuit board 3 and having been plated, a solder eutectic paste of 36Pb-64Sn (melting point is about 183 °C) is printed by using a metal mask (not shown) and in such a manner as to cover the pad 17 entirely, whereby to form a paste layer 21. In the meantime, the pad 17 is about 150  $\mu\text{m}$  in diameter, the opening diameter of the metal screen is 200  $\mu\text{m}$ , and the thickness of the mask is 70  $\mu\text{m}$ .

(4) Then, a flattening and leveling jig 23 is set to cover all of the paste layers 21. The flattening and leveling jig 23 is made of, for example, ceramic such as silicon nitride and having a control portion 23a in the form of a flat or planar plate and of such a length extending over the paste layers 21 and leg portions 23b disposed at the opposite ends of the control portion 23a and having the same height. The flattening and leveling jig 23 is thus constructed to have a U-like cross section. The bottom surface (planar surface) 23c of the recessed portion of the flattening and leveling jig 23 is ground accurately so as to be 0.1  $\mu\text{m}/\text{mm}$  in the flatness.

The length (height) of the leg portions 23b is set so that the planar surface 23c is put in contact with the upper surface of the paste layer 21 or a little distant from same ( $h = 50 \mu\text{m}$ , for instance). That is, the length is set so as to control or adjust the height of the top of the solder bump 1 to a predetermined value by making a mass of solder tending to become spherical when heated to melt and formed into a solder bump as will be described hereinafter, contact at the top with the planar surface 23c.

(5) Then, the circuit board 3 and the flattening and leveling jig 23 in the state of the latter being installed

on the former, is disposed in a furnace (not shown) for reflowing and are heated up to the temperature higher than the melting point (183 °C in this case) by 10 to 40 °C and thereafter cooled. By this, the circuit board 3 having the solder bumps 1 shown in Figs. 1A and 1B is completed.

In the meantime, the area in which the solder bumps 1 are formed is rectangular, and 12 mm long and 17.5 mm wide.

The flattened top of the solder bump 1 which was obtained by the above described method (i.e., the flattened portion of top) was 80 to 140  $\mu\text{m}$  in diameter. Further, the coplanarity of the solder bump was 7  $\mu\text{m}$  and its value per unit length was 0.33 ( $=7/21.2$ )  $\mu\text{m}/\text{mm}$ .

In the meantime, in case the flattening and leveling jig 23 was not used as heretofore, the coplanarity of the solder bump was 21  $\mu\text{m}$  and its value per unit length was 1.0  $\mu\text{m}/\text{mm}$ .

In this manner, according to the present invention, by disposing the flattening and leveling jig 23 having the control portion 23a and the leg portions 23b, at a predetermined position on the paste layers 21, the tops of the solder bumps 1 can be flattened and leveled all at once.

Further, the detection on the position of the top of the solder bump 1 can be easy, so there is produced such an effect in that the measurement of the coplanarity is simplified.

Furthermore, all of the tops of the solder bumps 1 are flattened and leveled by one planar surface 23C at the time when the solder is in a melted state, the coplanarity can be made small, and thus the joining property of a circuit board 3 and an integrated circuit chip or a printed circuit board can be made higher or improved, while it becomes



possible to perform the conduction test, insulation test, and the like assuredly.

Particularly, since flattened and leveled all at once by the planar surface 23C, the tops of the solder bumps are formed after the shape of the planar surface 23C, even if the circuit board is bent or curved for some reason, while allowing the difference in height of the pads 17 due to the warp or curvature of the substrate to be absorbed in the process of flattening and leveling which is carried out through melting of solder (refer to Fig. 2B). Accordingly, from this point, a pronounced effect that the coplanarity is lowered is produced.

Actually, in this example, it was observed that the warp or curvature of the circuit board 3 was about  $13\text{ }\mu\text{m}$  per 21.2 mm that was the maximum distance between the solder bumps 1. However, as mentioned above, the coplanarity of the solder bump 1 was restricted to  $7\text{ }\mu\text{m}$ , so it will be seen that this example makes it possible to absorb the warp or curvature of the circuit board 3 and make lower the coplanarity.

Further, only by changing the height of the leg portions 23b of the flattening and leveling jig 23, it becomes possible to set the height of the solder bump 1 to a desired value with ease.

In the meantime, when the circuit board 3 produced in the above described manner by using the flattening and leveling jig 23 was heated again to reflow the solder bumps, the reflowed solder bumps became spherical by the effect of the surface tension so that the flattened portions at the tops thereof were lost while the tops (the highest portion) increased in height. The variation was that the height of  $45\text{ to }55\text{ }\mu\text{m}$  before heating varied to  $75\text{ to }105$

μm after heating, so increase in height of 30 to 50 μm was observed with respect to each solder bump.

This shows that when the circuit board 3 of this example and its mating integrated circuit chip or printed circuit board are placed on upon another for joining thereof the both can be joined favorably even if there are some pairs of solder bumps 1 and their joining objects (i.e., pads or the like) which are out of contact from each other due to the warp or the like of the joining or mating object of the circuit board 3. This is because when the solder is heated to reflow the tops of the solder bumps 1 become higher and are made to contact the mating pads.

Accordingly, speaking with respect to the above described example, if the variation in the curvature or height in the area where the mating pads to be joined are formed is equal to or smaller than 30 μm, joining of the pads to the circuit board 3 can be done favorably by absorbing the variations in the positions of the mating pads in the direction of the height thereof, so it will be understood that the circuit board 3 is quite excellent in the joining ability.

For the characteristics of the solder bumps 1 it is desired that the height of the tops increases as large as possible, and further for the purpose of lowering the insulation property it is desired that any solder ball and solder bridge that lower the insulation property or ability are not caused. To this end, it will do to make the diameter of the flattened surface of the solder bump 1 be equal to that of the pad 17, and it is further desirable to make the height of the solder bump 1 be smaller than the diameter of the pad 17.

### Example 2

Description will be made to example 2. By this example, the top of the solder bump is flattened by a press. In the meantime, description similar to that of example 1 will be omitted or simplified for brevity.

(1) By using the similar materials to example 1 and the processes similar to the above described processes (1) to (3) of same, masses of solder paste are applied to the respective pads on the circuit board by printing.

(2) The circuit board to which the masses of solder paste are applied by printing is disposed in a furnace for reflowing similarly to the conventional method and heated up to a temperature higher than the melting point of the solder by 10 to 40 °C and thereafter cooled. By this, a circuit board 33 having nearly spherical solder bumps 31 as shown in Figs. 3 and 4A is obtained.

(3) Then, the circuit board 33 having the solder bumps 31 is disposed in a lower jig 35 having a U-like cross section and made of stainless steel. In the meantime, the height of the solder bumps 31 is equal to the result of the depth of a recessed portion 35a of the lower jig 35 (e.g., 1.05 mm) minus the thickness of the circuit board 33 (e.g., 1.00 mm), so the height of the side wall 35b or the depth of the recessed portion 35a is set in proportion to the desired height of the solder bumps 31.

(4) Then, a stainless steel upper pressing plate 39 of a pressing device 37 is let to go downward to press the tops of the solder bumps 31 under pressure of 5kg/cm<sup>2</sup> for one minute and make them flattened. In the meantime, both of the upper pressing plate 39 and the recessed portion 35a of the lower jig 35 are of the flatness of 0.15 μm/mm.

By this, the tops of the solder bumps 31 having been nearly spherical before pressing as shown in Fig. 4A and having been 21  $\mu\text{m}$  in coplanarity were flattened as shown in Fig. 4B, so that a circuit board 33 having solder bumps 31 whose coplanarity was 10  $\mu\text{m}$  and whose coplanarity per unit length was 0.47  $\mu\text{m}/\text{mm}$  was obtained. In the meantime, this production method is characterized by fine wrinkles or folds formed in the peripheral portion of the solder bump 31 adjacent the top.

In this manner, according to the present invention, it becomes possible to form a plurality of solder bumps 31 whose tops are flattened, all at once by pressing the tops of the solder bumps 31 which have been once melted and formed into a spherical shape.

Due to this, similarly to example 1, an effect that measurement of the coplanarity is simplified can be produced. In the meantime, in the event that the circuit board 33 is warped or curved, the circuit board 33 is formed after the flat or planar surface of the recessed portion 35a and flattened. Then, when the upper pressing plate 39 is returned to its upper position, there may occur such a case in which the circuit board 33 recovers a little its warp or curvature. However, the coplanarity is still smaller than before, thus making it possible to improve the joining ability of the circuit board 33 while making it possible to perform the insulation test or the like assuredly.

Further, only by changing the depth of the recessed portion 35a of the lower jig 35, the height of the solder bump 31 can be set to a desired value with ease.

A still advantage of this example is that the work is easy since it can be fulfilled simply by pressing.

### Example 3

Example 3 will be described hereinafter. This example is similar in flattening the tops of the solder bumps by means of a press to the above described example 2 and differs in adding heat at the time of pressing. In the meantime, similar part of description to example 2 is omitted or simplified for brevity. Further, the same reference numerals are used.

(1) By way of the above described processes (1), (2) and (3) of example 2, the printed circuit board 33 having solder bumps 31 is accommodated in the lower jig 35 as shown in Fig. 3.

(2) Then, the pressing device 37 and the lower jig 35 are surrounded by a heat-insulating material so as to be within an enclosed space through which nitrogen gas is made to flow at the flow rate of 100 liter/min. Under this condition, the pressing upper plate 39 heated up to about 200 °C is let to go downward to press the tops of the solder bumps 31 with a pressing pressure of 5 Kg/cm<sup>2</sup> for one minute while heating and softening the same for thereby flattening the tops. In the meantime, a heater (not shown) is disposed inside the pressing upper plate 39 so that the pressing upper plate 39 is heated by the heater so as to be held at a temperature higher than the melting point of the solder by 20 to 60.

By this, the tops of the solder bumps 31 were depressed or flattened as shown in Fig. 4A, and the printed circuit board 33 having the solder bumps 31 whose coplanarity was 7 μm and whose coplanarity per unit length was 0.33 μm/mm, as shown in Fig. 4C, was obtained.

In the meantime, this production method is characterized in that the periphery of the solder bump 31

adjacent the top is not formed with such fine wrinkles or folds as in example 2.

5 In this manner, by this example, it becomes possible to form a plurality of solder bumps 31 whose tops are flattened and whose peripheries adjacent the tops have no wrinkles or folds by pressing the solder bumps 31 which have been made to melt once and became spherical, all at once by means of the pressing upper plate 39 heated up to a temperature higher than the melting point of the solder.

10 For this reason, the example 3 can produce substantially the same effect as the example 2 and can make the coplanarity quite smaller similarly to the example 1 since the solder bumps 31 are heated and then flattened.

15 Further, since the solder bumps 31 are heated and pressed to be flattened, it becomes possible to prevent oxidation due to stress or strain resulting from pressing while being possible to prevent oxidation by heating since nitrogen gas or the like inactive gas is let to flow at the time of pressing.

#### 20 Example 4

Example 4 is for flattening the top of the solder bump by surface grinding. In the meantime, similar description to example 1 will be omitted or simplified for brevity.

25 (1) By using similar materials to example 1 and processes similar to the processes (1), (2) and (3) of same, a solder paste is applied to a circuit board by printing.

(2) Then, the circuit board to which solder paste is applied by printing is disposed in a furnace for reflowing, 30 similarly to the conventional method and heated up to a temperature higher than the melting point of the solder by 10 to 40 °C and thereafter cooled. By this, a circuit board

43 having nearly spherical solder bumps 41 as shown in Fig. 5 is obtained.

(3) Then, the circuit board 43 having such solder bumps 41 is placed on a sucking plate (i.e., a plate to which an object is adhered by suction) 47 and adhered thereto by suction by decreasing the atmospheric pressure on the lower side of the sucking plate.

(4) Then, a grinding wheel 51 of a grinding machine 49, specifically, an abrasive disk of the grain size of 1000 and of the flatness of  $0.2 \mu\text{m}/\text{mm}$  is let to go downward at the speed of  $0.2 \text{ mm}/\text{sec}$  whilst being driven to rotate at the speed of 120 rpm, whereby to grind and make flat and leveled the tops of the solder bumps 41. In this example, for the circuit board which was 1 mm thick, the grinding wheel 51 was let to go down to the level which was 1.05 mm distant from the upper surface of the sucking plate 47.

By this, a circuit board 43 having solder bumps 41 whose coplanarity was  $10 \mu\text{m}$  and whose coplanarity per unit length was  $0.47 \mu\text{m}/\text{mm}$  was obtained through grinding of the solder bumps 41 which, before being ground, was nearly spherical and whose coplanarity was  $30 \mu\text{m}$ .

In this manner, according to the present invention, it becomes possible to form a plurality of solder bumps 41 whose tops are flattened, all at once by grinding the tops of the solder bumps 41 having been once molten and become spherical.

For this reason, this example can produce substantially the same effect as example 2, and has an advantage that by simply setting the position to which the grinding wheel 51 is let to go down the height of the solder bump 41 and the diameter of the flat portion at the top can be changed or altered with ease.

In the meantime, although either of the dry type or wet type grinding method can be used in this example, either of them requires to clean or wash the printed circuit board after grinding since ground metal particles and the like  
5 adhere or stick to the surface of the printed circuit board in either method.

#### Example 5

In this example, description will be made only to a flattening and leveling jig for use in manufacturing a  
10 circuit board having solder bumps. In the meantime, similar description to example 1 will be omitted or simplified for brevity.

As shown in Fig. 12, a flattening and leveling jig  
15 61 used for this example is constructed of a control member 63 in the form of a flat plate and a pair of leg members 65 disposed oppositely on the lower side of the control member 63.

The above described control member 63 is an alumina ceramic plate which is 25 mm square and 2 mm thick, and its  
20 one side surface (a surface used for flattening tops of solder bumps, and a lower surface in Fig. 12A) is grounded. The grounded side surface 63a is formed with a pair of grooves 63b which is 25 mm long, 0.4 mm wide and 0.25 mm deep, at locations about 2 mm distant from the opposite  
25 ends, respectively.

The leg members 65b are fitted in the grooves 63b in such a manner as to be buried half and are constituted by a round stainless steel wire of 0.3 mm in diameter. In the meantime, it is desired to bend the opposite ends of the  
30 stainless steel wire upward and inward of the control member 63 as shown in Fig. 12C for the purpose of preventing removal of the leg members 65 from the control member 63.



In the structure in which the leg members 65 are fitted in the grooves 63b, the leg members 65 are adapted to protrude a little ( $50\text{ }\mu\text{m}$ ) from the planar surface 63a, so it becomes possible to set the distance between the control member 63 and the circuit board (i.e., the height of solder bump) to  $50\text{ }\mu\text{m}$ , i.e.,  $0.3\text{ mm}$  (diameter of stainless steel wire) minus  $0.25\text{ mm}$  (depth of groove).

The flattening and leveling jig 61 used in this example is constructed so that the control member 63 and the leg members 65 which are independent constituent parts, so its manufacture is easy since it does not require machining of an alumina ceramic flat plate which is a material quite difficult of being machined, for forming the alumina ceramic flat plate into such a shape that the legs 65 protrude from the flat plate 63, but only requires cutting of grooves 63, so the machining of the jigs 61 is easy.

Particularly, in this example, the surface 63a used for pressing the tops of the solder bumps is constituted by the planar surface of the plat member, so machining for making the surface 63a flat or planar is easy and furthermore its flatness is high. For this reason, this example can make the coplanarity smaller.

Test was conducted with respect to example 5. In this test, a flattening and leveling jig having a control member made of alumina ceramic and leg members made of stainless steel wire which were independent constituent parts as in example 5 was produced, while producing a flattening and leveling jig made of alumina ceramic in which a control member and leg members were integral with each other as a comparative example, and by using them flattening of the tops of solder bumps was actually performed.

By this test, it was revealed that in case of the example of this invention the flatness was  $0.05 \mu\text{m/mm}$ , days required for manufacture were three days and the coplanarity of solder bumps was  $0.2 \mu\text{m/mm}$ , i.e., the jig of this example was favorable since its manufacture was easy and the coplanarity was small. However, in case of the comparative example, the flatness was  $0.10 \mu\text{m/mm}$ , 6 days required for manufacture were six days and the coplanarity of solder bumps was  $0.4 \mu\text{m/mm}$ , so the comparative example was not favorable since its manufacture was difficult and the coplanarity was large. Furthermore, in case of the comparative example, its cost (manufacturing cost of the flattening and leveling jig) was twice as high as that of the example of this invention.

In the meantime, while in the above described examples the grooves are formed in a control member for fittingly receive therein the leg members, it will do not to form the grooves in case the height of the leg members is large to some extent (e.g., 0.3 mm or more) but to dispose the stainless steel wire just on the lower side of the control member 71 to serve as the leg members as shown in Fig. 14.

In this instance, since it is not required to form the grooves, the flattening and leveling jig can be produced more easily. In the meantime, by changing the diameter of the stainless steel wire, the height of the solder bumps can be set freely.

The present invention is not limited to the above described examples but various modifications and variations may be made thereto without departing from the subject matter of this invention.

(1) For example, as a material for a substrate of a printed circuit board, it can be employed other than plastics (resin), ceramics such as alumina or the like, a composite material comprised of resin and glass fiber or the like, a composite material comprised of resin and ceramics or the like.

(2) In the above described examples, description is made as to solder bumps for joining an integrated circuit chip to a circuit board by flip-chip technology. However, this invention is not limited to this but can be applied to such solder bumps for joining the circuit board to a printed circuit board such as motherboard or to a BGA substrate in which solder bumps are disposed so as to form a grid pattern or checkered pattern.

(3) The solder used can be of any type such as a high melting point solder containing 90% Pb and a solder containing Ag or In, which is selected depending upon usage. Further, the flux contained in the solder can be any one of the R type, RMA type and RA type ( in the order of smaller reduction ability or property). In the meantime, the material of the bumps herein used can be, other than Pb-Sn solder which is usually called soft solder, Au-Sn alloy, Au-Si alloy or the like.

(4) The technology used for applying the solder material to the pads, can be, other than the above described technology of printing of paste, a technology of dropping solder paste by the use of a dispenser, a technology of mounting a preform, pellet and solder balls, or the like.

As having been described above, the circuit board of this invention has solder bumps whose tops are flattened. Accordingly, it becomes possible to make smaller the coplanarity of the solder bumps and improve the joining

ability of the printed circuit board. Further, a pronounced effect of this invention is that the examination or inspection about the insulation or the like can be done with efficiency and measurement of the coplanarity can be  
5 simplified

Further, a method of producing a circuit board having solder bumps according to the present invention, can produce an excellent effect that the circuit board having the above described excellent characteristics can be  
10 produced with ease by a simple step of melting the solder and pressing the same after cooling, which step is performed by using a control member, or by a simple step of grinding the solder after molted and cooled.

Particularly, in case the solder is melted by using  
15 a control member, there results an excellent advantage, i.e., decreased coplanarity, simplified manufacturing steps, prevention of solder bump oxidation, etc.

Further, the flattening and leveling jig of this invention can be produced with ease even when a material  
20 which has a difficulty in machining but is suitable for use in flattening the tops of the solder bumps, is used, thus making it possible to reduce the manufacturing cost in manufacture of a circuit board having solder bumps.

Further, cutting or forming a flat or planar surface on the  
25 control member can be done with ease, thus making it possible to decrease the manufacturing cost of the flattening and leveling jig while making lower the coplanarity of the solder bumps.

30

**WHAT IS CLAIMED IS:**

1. A circuit board comprising:  
a substrate having a joining surface; and  
a plurality of solder bumps disposed on said joining  
5 surface of said substrate in such a manner as to form a  
predetermined profiled line or surface pattern;  
wherein said solder bumps have tops which are flat  
and leveled, and a coplanarity of said solder bumps is 0.5  
 $\mu\text{m}$  or less per 1 mm.  
10
2. A circuit board according to claim 1, further  
comprising circular pads interposed between said solder  
bumps and said substrate to serve as base layers of said  
solder bumps.  
15
3. A circuit board according to claim 2, wherein said  
tops of said solder bumps have nearly circular flat surfaces  
which are smaller in diameter than said pads.
- 20 4. A circuit board according to claim 2, wherein said  
tops of said solder bumps have nearly circular flat surfaces  
which are substantially equal in diameter to said pads, and  
the height of said solder bumps is smaller than the diameter  
of said pads.
- 25 5. A method of producing a circuit board including a  
substrate having a joining surface, and a plurality of  
solder bumps disposed on the joining surface of the  
substrate in such a manner as to form a predetermined  
30 profiled line or surface pattern, wherein the solder bumps  
have tops which are flat and leveled, and a coplanarity of

the solder bumps is 0.5  $\mu\text{m}$  or less per 1 mm, the method comprising the steps of:

placing masses of solder on said solder bumps, respectively;

5 disposing a control member in the form of a flat plate at a predetermined position above said masses of solder; and

forming said masses of solder into said solder bumps all at once by melting said masses of solder and allowing  
10 said control member to control the height of said solder bumps while flattening said tops of said solder bumps all at once.

6. The method according to claim 5, wherein pads are  
15 disposed on said joining surface of said substrate in such a manner as to form said profiled line or surface pattern, and said solder bumps are once formed on said pads, respectively and then pressed in such a manner as to allow said tops to become flat and leveled.

20 7. The method according to claim 5, wherein pads are disposed on said joining surface of said substrate in such a manner as to form said profiled line or surface pattern, and said solder bumps are once formed on said pads,  
25 respectively and then ground in such a manner as to allow said tops to be flattened and leveled.

8. A flattening and leveling jig for disposition above  
30 masses of solder mounted on a main surface of a circuit board for controlling the height of solder bumps into which the masses of solder are formed by being heated and melted, the jig comprising:

a control member having a planar surface for controlling the height of said solder bumps; and

a pair of leg members which are independent parts and disposed on the side of said planar surface of said control member for support of said control member and for positioning of said planar surface.

9. The flattening and leveling jig according to claim 8, wherein said leg members are so constructed and arranged as to allow said planar surface of said control member to be parallel to said main surface of said substrate when said flattening and leveling jig is disposed in place.

10. The flattening and leveling jig according to claim 9, wherein said leg members are made of wire.

11. The flattening and leveling jig according to claim 10, wherein said control member has on the side of said planar surface a pair of groove in which said leg members are fitted.

25

30

**ABSTRACT OF THE DISCLOSURE**

A circuit board having a plurality of solder bumps is provided. The solder bumps are flattened and leveled at the tops so that the coplanarity of the solder bumps is 0.5  $\mu\text{m}$  or less per 1 mm. The flattened and leveled tops of the solder bumps are formed by cold pressing, hot pressing or grinding. Method of forming such solder bumps and jigs used for carrying out such methods are also provided.

10

15

20



FIG.1A

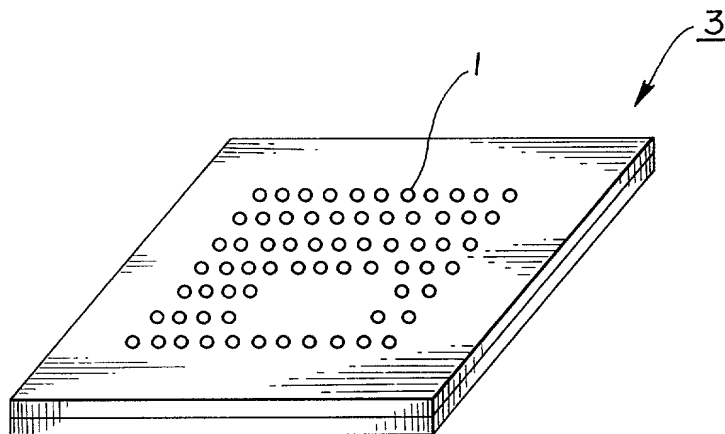
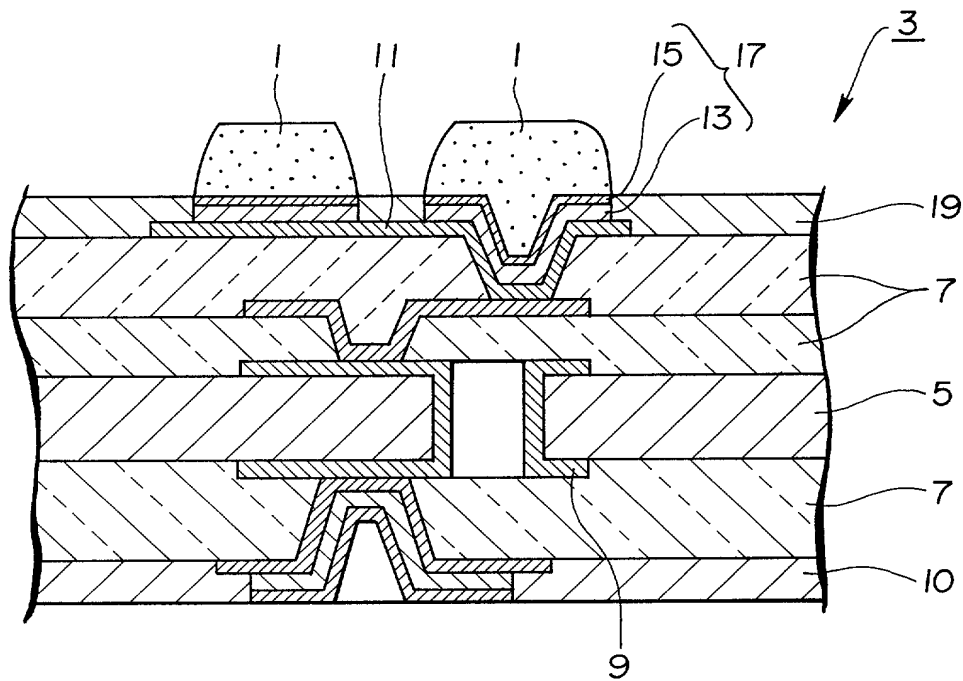
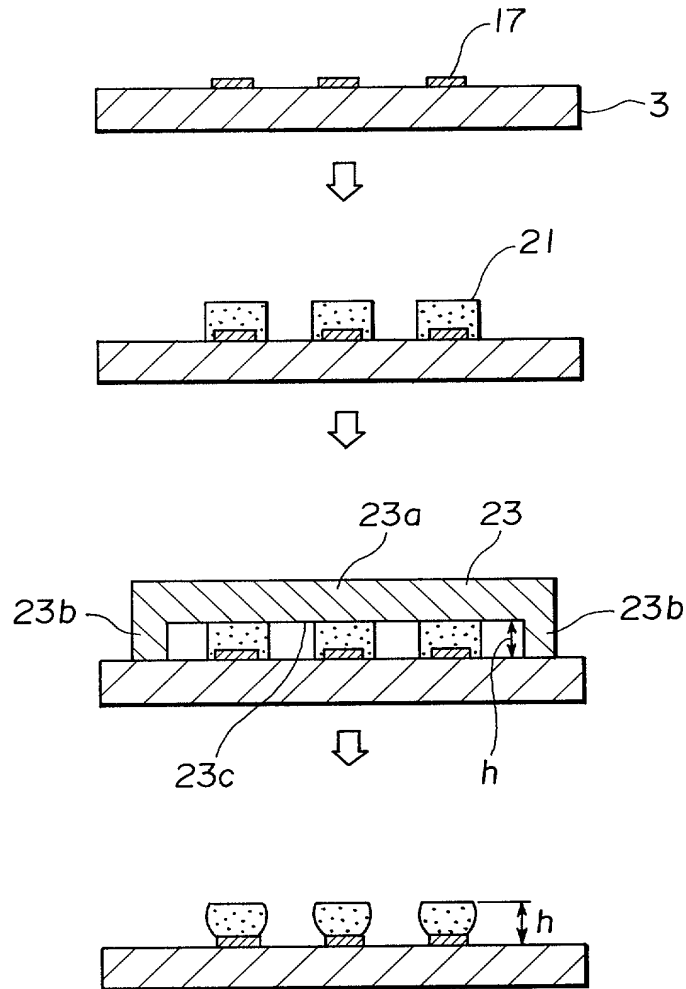


FIG.1B



**FIG.2A**



**FIG.2B**

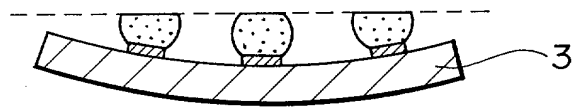
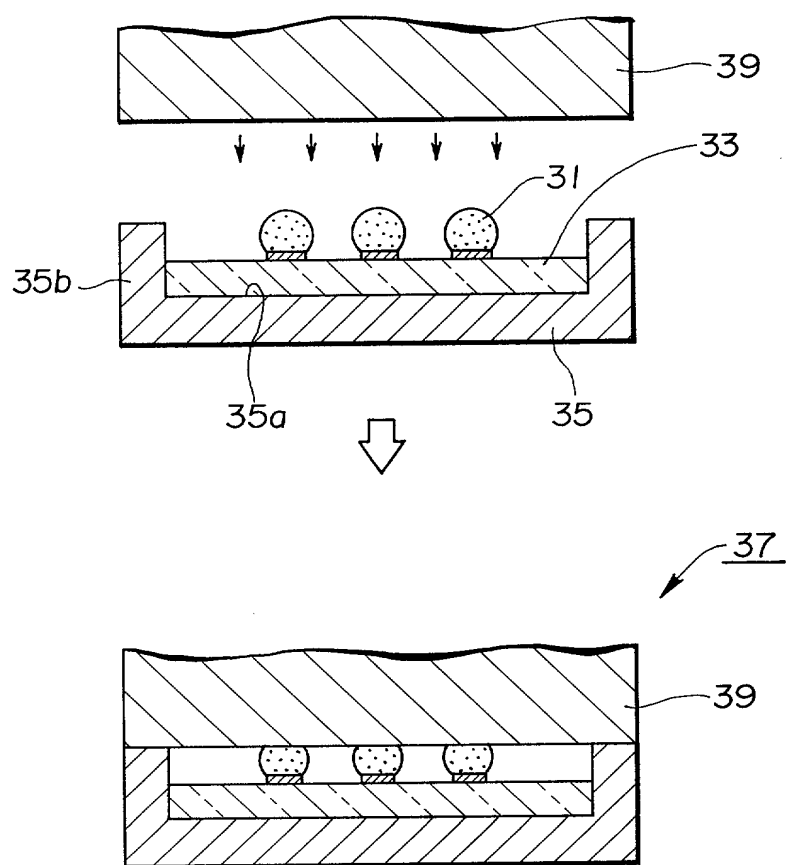
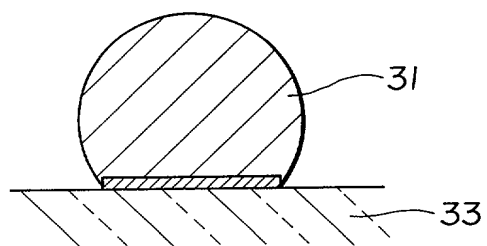


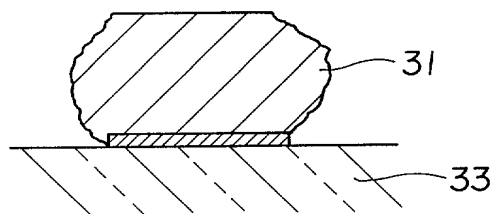
FIG.3



**FIG.4A**



**FIG.4B**



**FIG.4C**

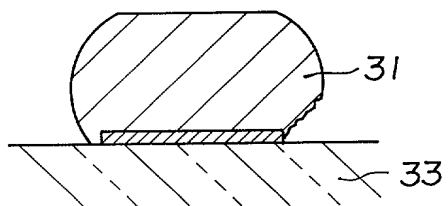


FIG.5

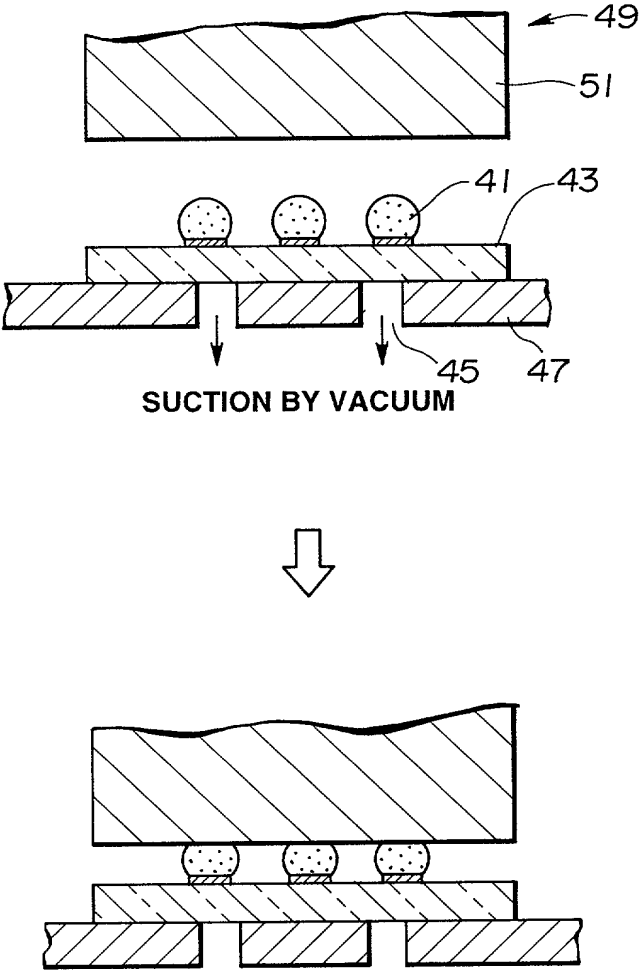


FIG.6

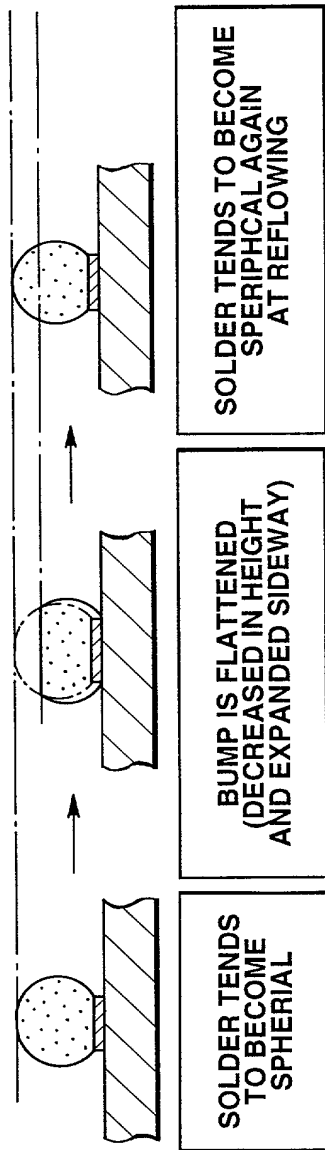


FIG.7

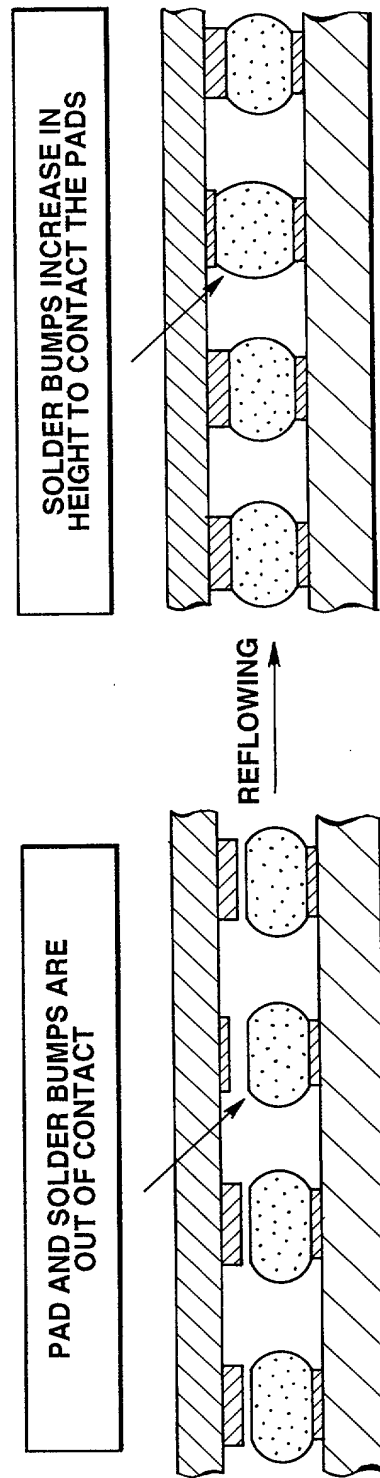


FIG.8

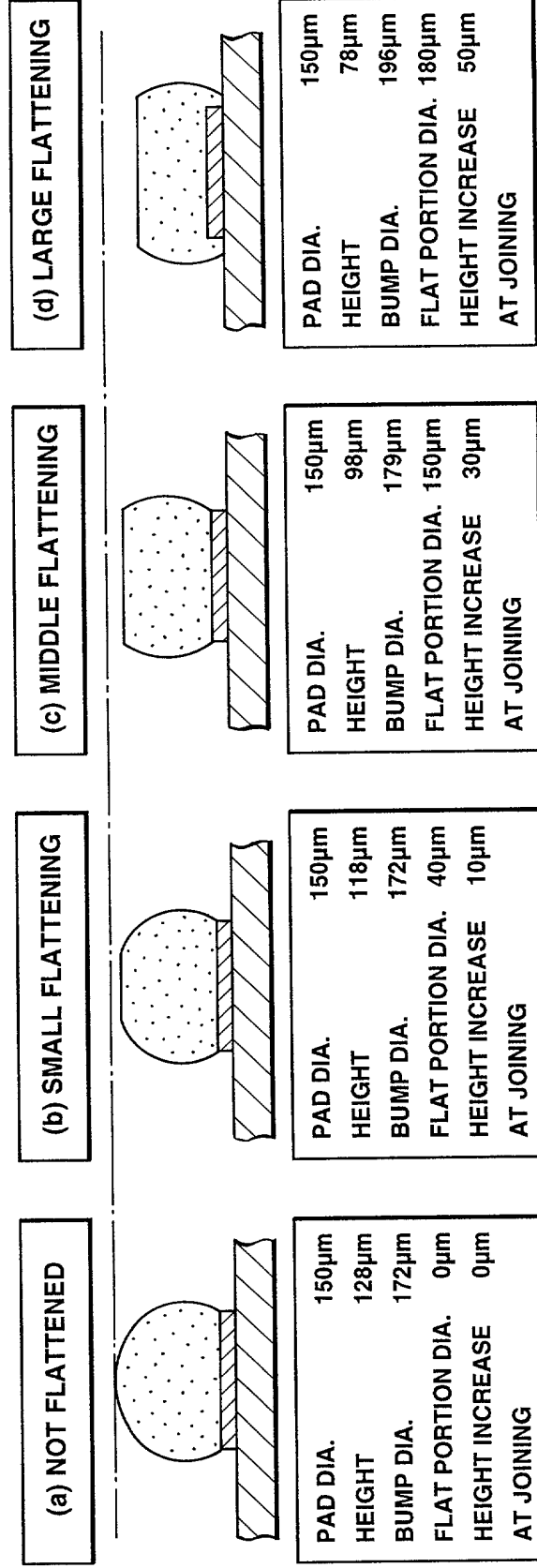


FIG.9

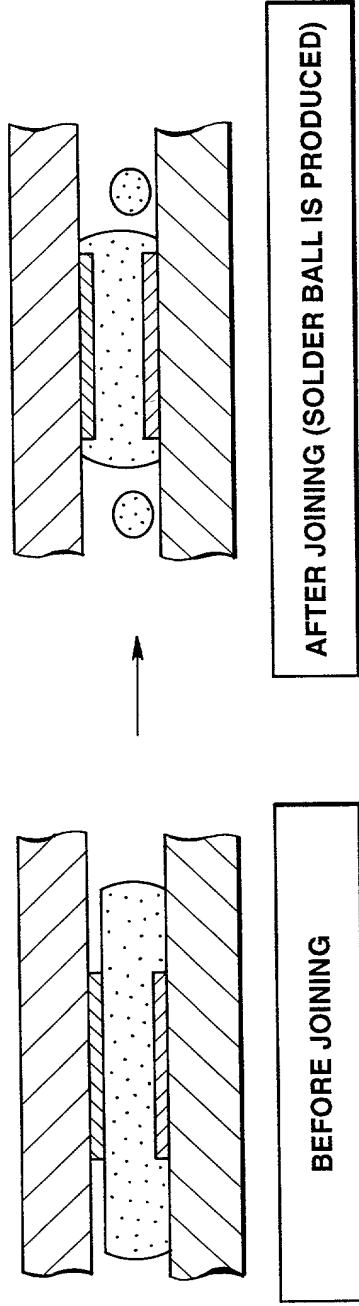


FIG.10

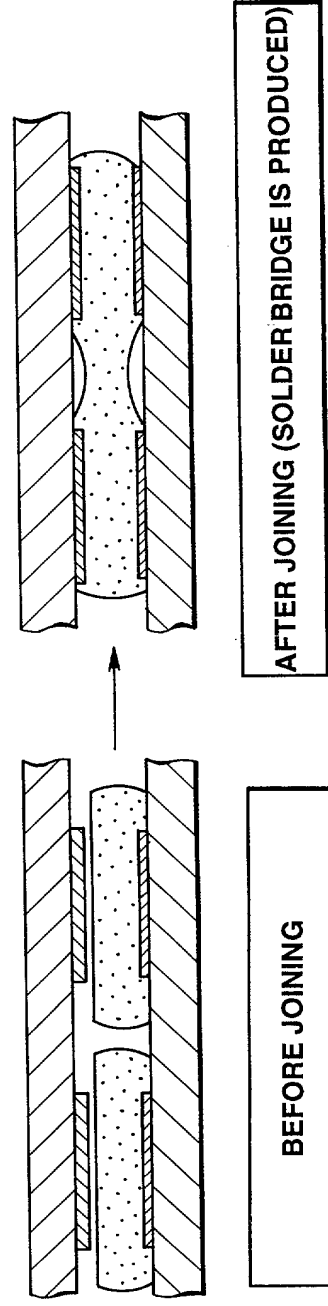




FIG.11A

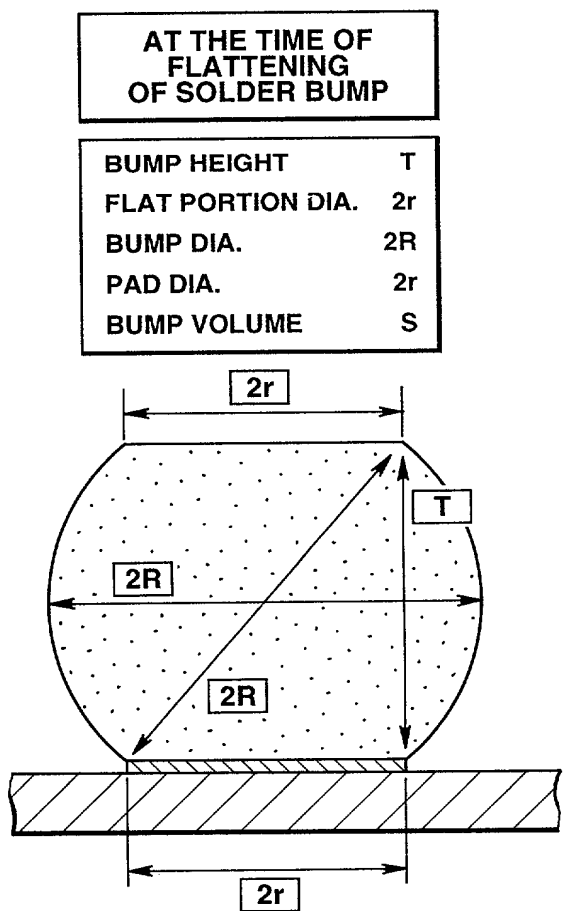
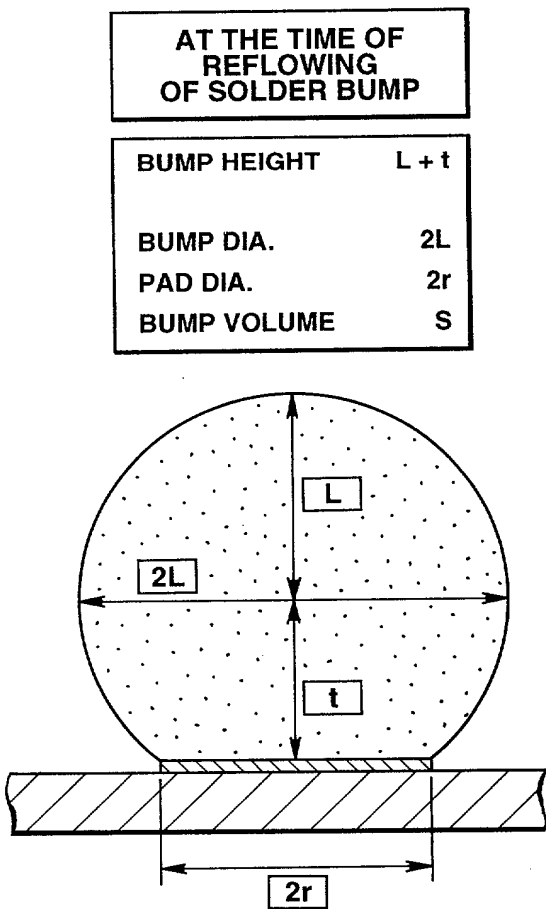
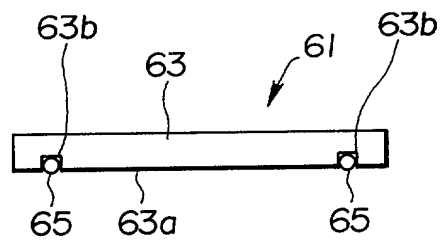


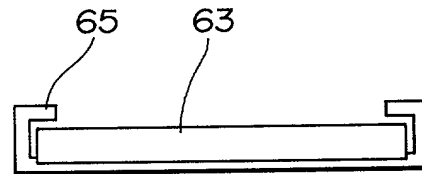
FIG.11B



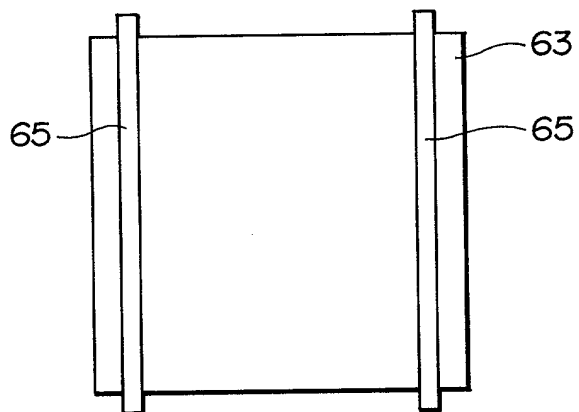
**FIG.12A**



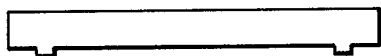
**FIG.12C**



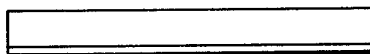
**FIG.12B**



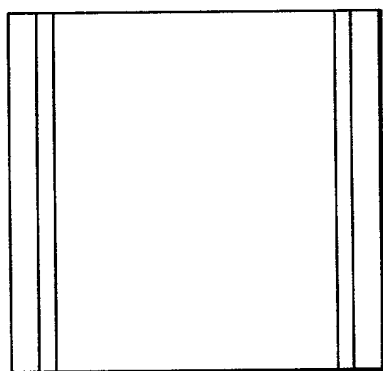
**FIG.13A**



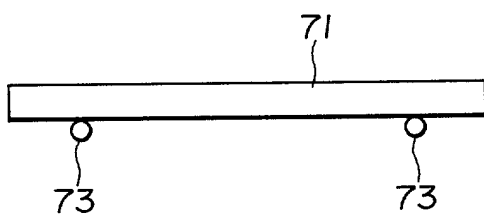
**FIG.13C**



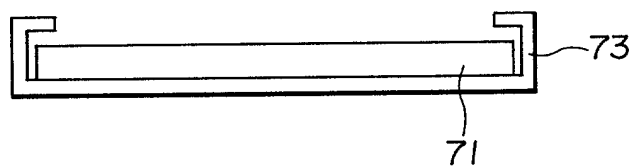
**FIG.13B**



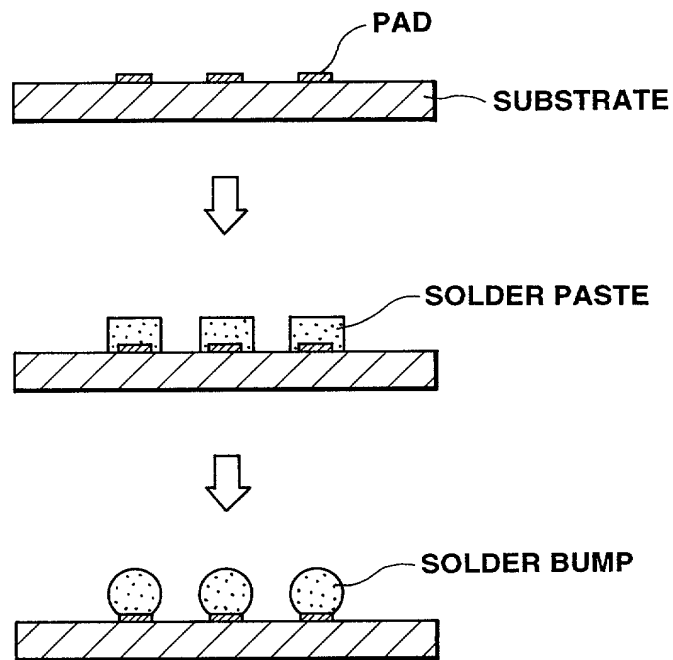
**FIG.14A**



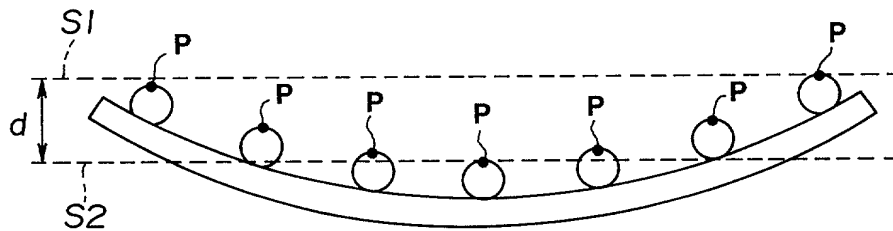
**FIG.14B**



**FIG.15A**



**FIG.15B**



# DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

IMPROVEMENT IN OR RELATING TO CIRCUIT BOARD HAVING SOLDER BUMPS  
the specification of which (check one)

☒ is attached hereto

☐ was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

## PRIOR FOREIGN APPLICATION(S)

NUMBER	COUNTRY	DAY/MONTH/YEAR FILED	PRIORITY CLAIMED
8-212845	Japan	12 August 1996	Yes
8-76960	Japan	29 March 1996	Yes
8-108287	Japan	26 April 1996	Yes

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NO.	FILING DATE	STATUS: PATENTED, PENDING, ABANDONED

I hereby appoint as my attorneys, with full powers of substitution and revocation, to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Stephen A. Bent, Reg. No. 29,768; David A. Blumenthal, Reg. No. 26,257; Joseph D. Evans, Reg. No. 26,269; John J. Feldhaus, Reg. No. 28,822; Donald D. Jeffery, Reg. No. 19,980; Peter G. Mack, Reg. No. 26,001; Bernhard D. Saxe, Reg. No. 28,665; Richard L. Schwaab, Reg. No. 25,479; Arthur Schwartz, Reg. No. 22,115.

Send all correspondence to **FOLEY & LARDNER**, 3000 K Street, N.W., Suite 500, P.O. Box 25696, Washington, DC 20007-8696.  
Address telephone communications to \_\_\_\_\_ at (202) 672-5300.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole Inventor Haruhiko MURATA	Signature of First or Sole Inventor <i>Haruhiko Murata</i>	Date 3/17/1997
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Post Office Address c/o NGK Spark Plug Co., Ltd. 14-18, Takatsuji-cho, Mizuho-ku, Nagoya-shi, Aichi 467 JAPAN		

Signatures should confirm to names as typewritten. ☒ Additional inventors on attached Page 2.

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Full Name of Third Inventor Masashi INAISHI	Signature of Third Inventor <i>Masashi Inaishi</i>	Date 3/17/1997
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Full Name of Fourth Inventor	Signature of Fourth Inventor	Date
Residence Address	Country of Citizenship	
Post Office Address		

Full Name of Fifth Inventor	Signature of Fifth Inventor	Date
Residence Address	Country of Citizenship	
Post Office Address		

Full Name of Six Inventor	Signature of Six Inventor	Date
Residence Address	Country of Citizenship	
Post Office Address		

Full Name of Seventh Inventor	Signature of Seventh Inventor	Date
Residence Address	Country of Citizenship	
Post Office Address		